Semiconductor Substrates

Single-crystal silicon is the enabling material of the Information Age just as steel was the enabling material of the Industrial Revolution.
Silicon (Si) is the “work horse” of the Microelectronics industry; Si is in Column (IV) of the periodic table and is an elemental semiconductor; GaAs is a (III-V) material and is a compound semiconductor.
Semiconductor Basics

**Resistance**

By Ohm’s Law, this is the ratio of the voltage across a device to the current flowing through: \( R = \frac{V}{I} \).

**Resistivity** (inverse of conductivity)

This is a parameter measured in \( \Omega \text{–m} \) that is helpful when comparing electrical properties of materials.
Silicon (Si) as a Substrate

Silicon is used almost exclusively in the fabrication of semiconductor devices even though many elements exhibit semiconducting properties.

Reasons:
• Silicon is an *elemental semiconductor*. Elemental semiconductors may be subjected to a large variety of processing steps without decomposition.
• Silicon has a *wider energy gap* (1.1 eV) than Ge (0.67 eV) and can operate at higher temperatures (~125-175°C).
• It is easy to protect the surface with a layer of silicon dioxide (SiO₂). Si has a *native oxide* layer of 1.5-2.0 nm that grows when exposed to air.
Useful Terms

Material classifications:

*Single crystal* – atoms occupy specific positions on the lattice
*Polycrystalline* – multiple single crystals randomly oriented
*Amorphous* – atoms have no long range order

The *phase diagram* is the map of a material in terms of solid/liquid phases for specific temperatures.

*Solid Solubility*: the maximum concentration of an impurity that can be dissolved in another material under equilibrium conditions.
Crystal: an array of repeated unit cells

Miller Indices – a way of identifying crystal planes (e.g. cube face, face diagonal, body diagonal)

Figure 2.5  (A) Common cubic crystals: simple cubic, body-centered cubic, and face-centered cubic. (B) Crystal orientations in the cubic system.
Silicon crystallizes in the diamond structure

FCC with 4 additional *interior* atoms

Dark atoms are highlighting corners, faces, and just one of the additional atoms

Figure 2.6  The diamond structure.
Crystal Defects: any interruption in the periodic lattice

Point defects

• vacancies: lattice sites where atoms are missing
• interstitials: atom occupies a space between occupied sites or an atom located in between atoms (self-interstitial)
• substitutional: foreign atoms occupy lattice sites normally occupied by Si

Line, dislocation defects

• edge dislocation: insertion of an extra line of atoms into a regular crystal causing crystal to distort
• screw dislocation: formed by the motion of one part of a crystal with respect to another

Area defects: stacking faults - extra plane of atoms; grain boundaries

Bulk defects – 3D irregularities, precipitates; not suited for fabrication of devices
Crystal Growth

Silicon wafer diameter used in manufacturing today is **300 mm or 12 inches**

Single crystal Si is grown primarily by

- **Czochralski (CZ) process** – involves solidification of a crystal from a melt; electronic grade polysilicon refined from quartzite ($\text{SiO}_2$) until it is very pure as the starting material.
CZ Method

A method for producing a large ingot (boule) of single crystal Si from a seed that is pulled and rotated from molten Si held in a crucible located in a chamber back filled with inert gas.
A picture of a 200 mm Si crystal as they are grown for chip manufacture in 2000.

Note that this huge crystal is hanging on a rather thin Si seed crystal.

This seed crystal has to not only support the weight of the crystal, but also the torque needed to rotate the crystal during its growth.

From the "Smithsonian", Jan 2000, Vol. 30, No. 10
Wafer Preparation

After growing the boule, the seed and tail are cut off and the boule is trimmed to the proper diameter. Either a flat (smaller wafers) or a notch (larger wafers) is ground into the edge of the boule to identify crystal orientation. A chemical etch is done to remove damage from grinding and then the boule is sliced into wafers with some type of diamond blade. One or both sides receive mechanical polishing with a chemical slurry.
Silicon has 4 outer electrons that are shared between adjacent atoms called a *covalent bond*.

*Doping* is the process in which carriers (electrons or holes) are intentionally added to a semiconductor.

By controlling the amount of impurities, one can control the semiconductor resistivity. The impurities are called *donors* (if electrons are added) or *acceptors* (if holes are added).
**Doping**: intentionally introduce dopant atoms into the melt so that a particular resistivity wafer can be made.

Boron (B) has 3 valence electrons and so can “accept” electrons to form a *p-type material* (majority carriers are holes and minority carriers are electrons).
Cleanroom Classes

Cleanrooms are classified according to the number and size of particles per volume of air.

Large numbers like "class 100" or "class 1000" denote the number of sub-micron particles (or larger) per ft³. Small numbers specify the decimal logarithm of the number of particles 0.1 µm or larger permitted per m³ of air.

Ordinary room air is approximately class 1,000,000

<table>
<thead>
<tr>
<th>Class</th>
<th>maximum particles/ft³</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>≥0.1 µm</td>
</tr>
<tr>
<td>1</td>
<td>35</td>
</tr>
<tr>
<td>10</td>
<td>350</td>
</tr>
<tr>
<td>100</td>
<td>350</td>
</tr>
<tr>
<td>1,000</td>
<td></td>
</tr>
<tr>
<td>10,000</td>
<td></td>
</tr>
<tr>
<td>100,000</td>
<td></td>
</tr>
</tbody>
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UA Microfabrication Facility

- Photolithography
- E-beam evaporation
- Ion milling
- Sputtering
- Deep RIE
- Reactive Ion Etch (RIE)
Photolithography

Used for patterning

Spin photoresist on
Align wafer and mask
Expose wafer to UV light source
Development
Hard bake
Removal of photoresist
E-Beam Evaporation

A Physical Vapor Deposition (PVD) Method used to deposit metallic films or oxides
Sputtering

Another PVD method to deposit metals
Ion Milling

- Atomic bombardment of a substrate
- Precision etching of material and useful in creation of cross-sections
Reactive Ion Etching

• A chemical method to etch material not protected by a masking material
Figure 1.3  A simple resistor voltage divider. At left is a circuit representation: at right is a physical layout. The layers shown at right are resistor, contact, and low-resistance metal.
Planar Process

IC’s are made possible by the planar process

Simple example: p-n junction (diode)

1) Start with p-type Si wafer (substrate)

2) Form a layer of SiO$_2$ on top surface by thermal oxidation

3) Pattern the oxide layer with photolithography

4) Selectively introduce impurities into the Si by diffusion (or ion implantation)

5) Junction is formed, metallization to contact n, p regions
Figure 1.6  Cross section of an MOS transistor showing gate, source, drain, and substrate electrodes. The “1” and “2” indicate very heavy and very light dopings, respectively.